(12) UK Patent Application (19) GB (11) 2 283 857 (13) A

(43) Date of A Publication 17.05.1995

(21) Application No 9422471.4

(22) Date of Filing 08.11.1994

(30) Priority Data
(31) 08149858 (32) 10.11.1993 (33) US

(71) Applicant(s)
Hewlett-Packard Company

(Incorporated in USA - California)

3000 Hanover Street, Palo Alto, California 94304, United States of America

(72) Inventor(s)
Larry S. Metz
Gordon Motley

(74) Agent and/or Address for Service
Williams,Powell & Associates
34 Tavistock Street, LONDON, WC2E 7PB, United Kingdom

(51) INT CL$^6$
H01L 23/60 , H02H 9/04

(52) UK CL (Edition N )
H1K KGPE
H2H HAPC H23G H25G

(56) Documents Cited
US 4698655 A

(58) Field of Search
UK CL (Edition N ) H1K KGPE , H2H HAPC
INT CL$^6$ H01L , H02H
Online : WPI

# (54) Electrostatic discharge protection circuit

(57) An ESD protection circuit that uses the well-known SCR latchup effect present in CMOS processes to divert the ESD current pulse away from sensitive circuit structures. The circuit uses an inverter trigger device (40, 42), with a voltage divider (44, 46) on its output, to control the amount of voltage necessary to cause latchup. This feature enables the SCR (10) absorb a high current pulse on the CMOS pad structures (15) caused by an ESD event, while also preventing the circuit from latching when an ordinary CMOS voltage is applied to the pad while the circuit being protected is unpowered. The circuit insures that the SCR will latch independent of breakdown effects, while also allowing the threshold voltage at which latchup occurs to be adjusted into the circuit by varying the sizes of the two FETS (44, 46), used as the voltage divider, at the fabrication stage.

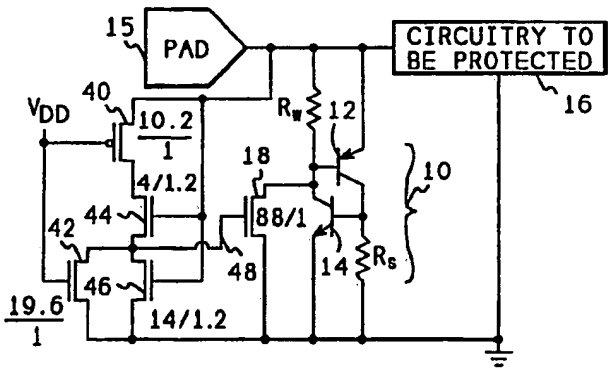


FIG. 4(a)

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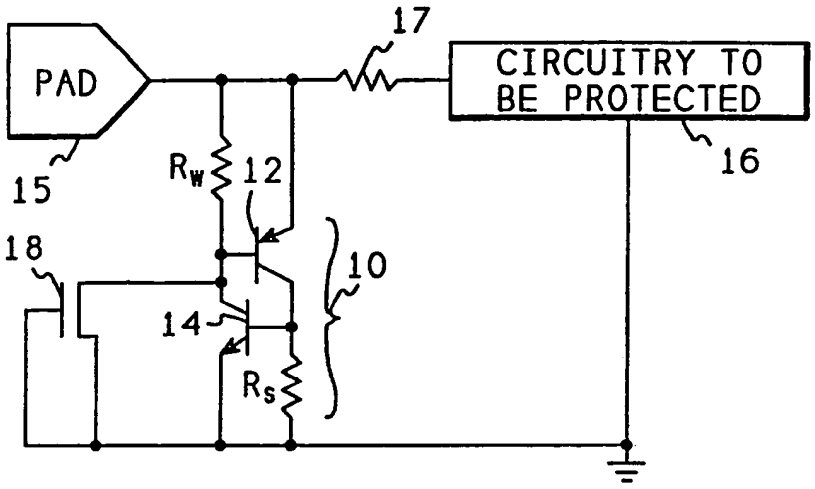
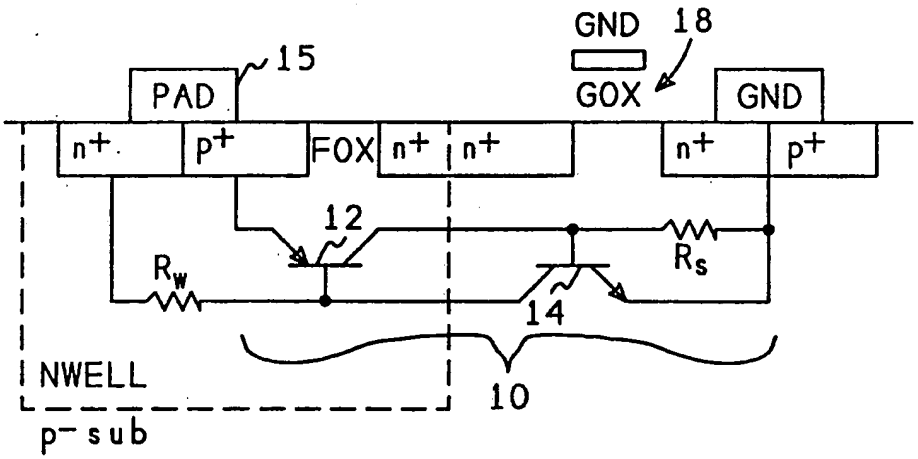


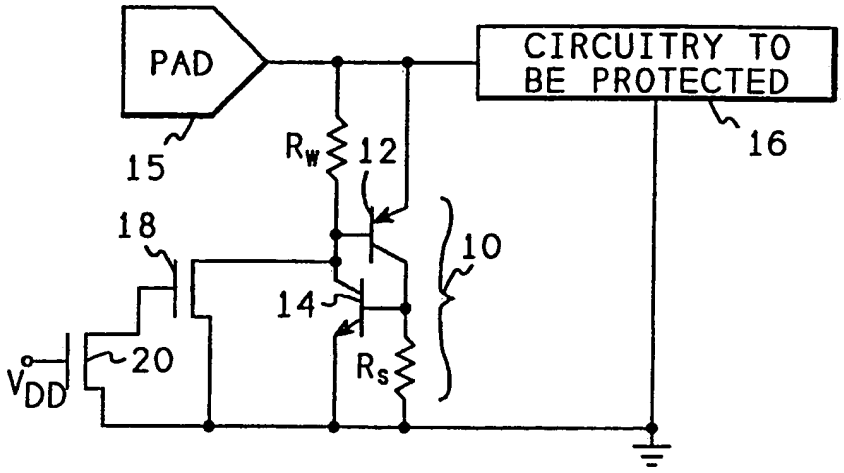

PRIOR ART

FIG. 1(a)



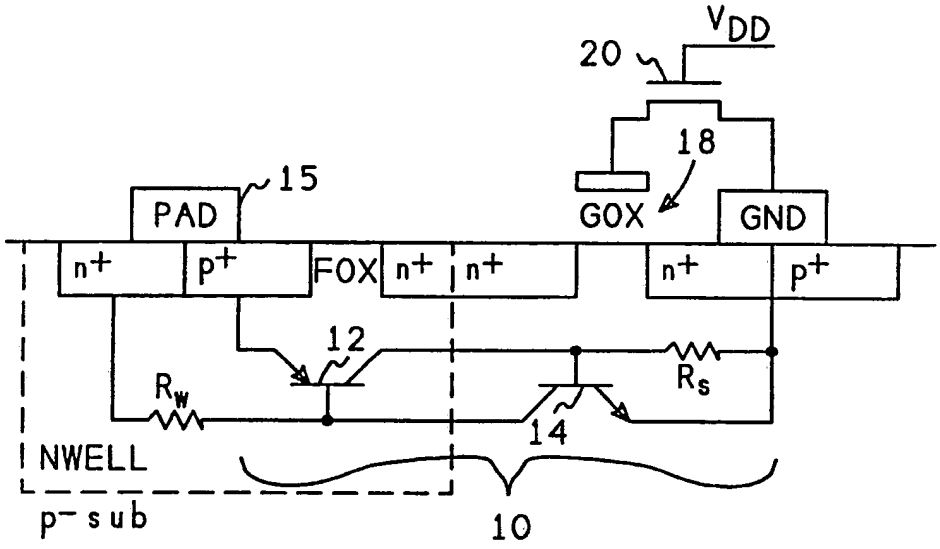

PRIOR ART

FIG. 1(b)




PRIOR ART

FIG. 2(a)




PRIOR ART

FIG. 2(b)

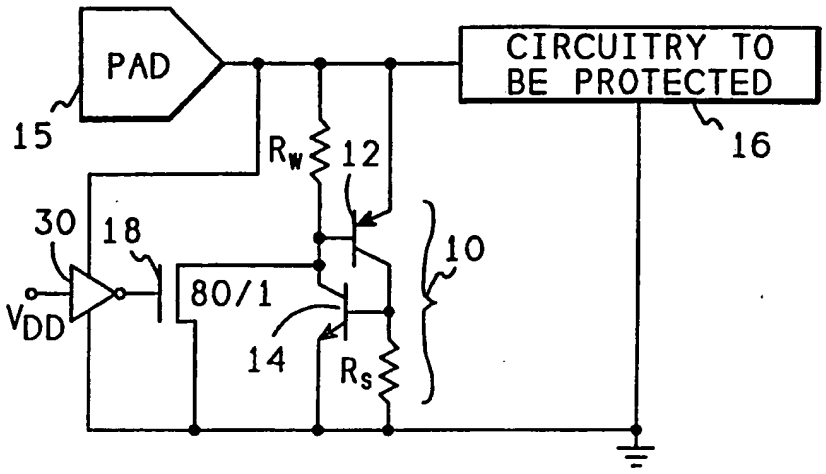

PAD
15
CIRCUITRY TO BE PROTECTED
16
$R_W$
12
30
18
10
80/1
$V_{DD}$
14
$R_S$

FIG. 3(a)

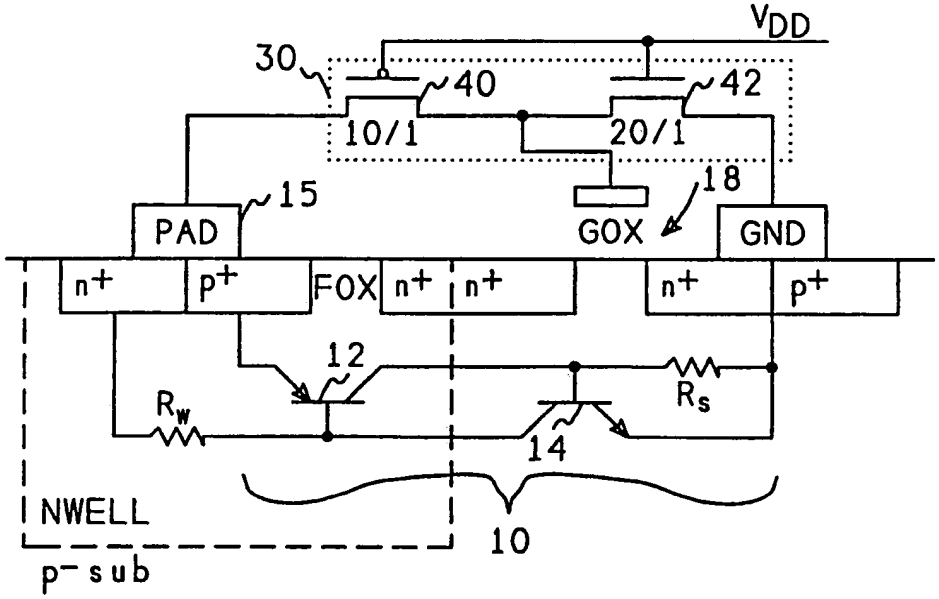

$V_{DD}$
30
40
42
10/1
20/1
18
15
PAD
GOX
GND
n+
p+
FOX
n+
n+
n+
p+
12
$R_W$
$R_S$
14
NWELL
10
p- sub

FIG. 3(b)

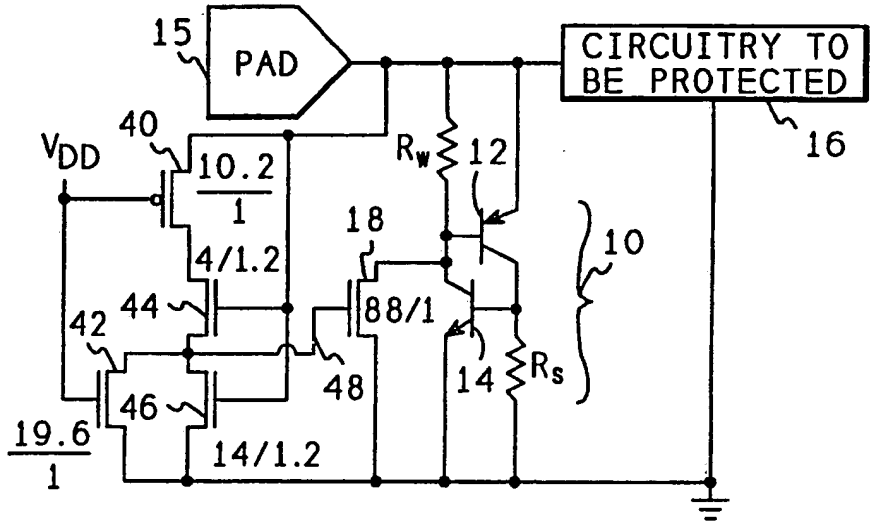

15
PAD
CIRCUITRY TO BE PROTECTED
16
40
$V_{DD}$
10.2/1
$R_w$
12
18
10
4/1.2
44
88/1
42
48
14
$R_s$
46
19.6/1
14/1.2

FIG. 4(a)

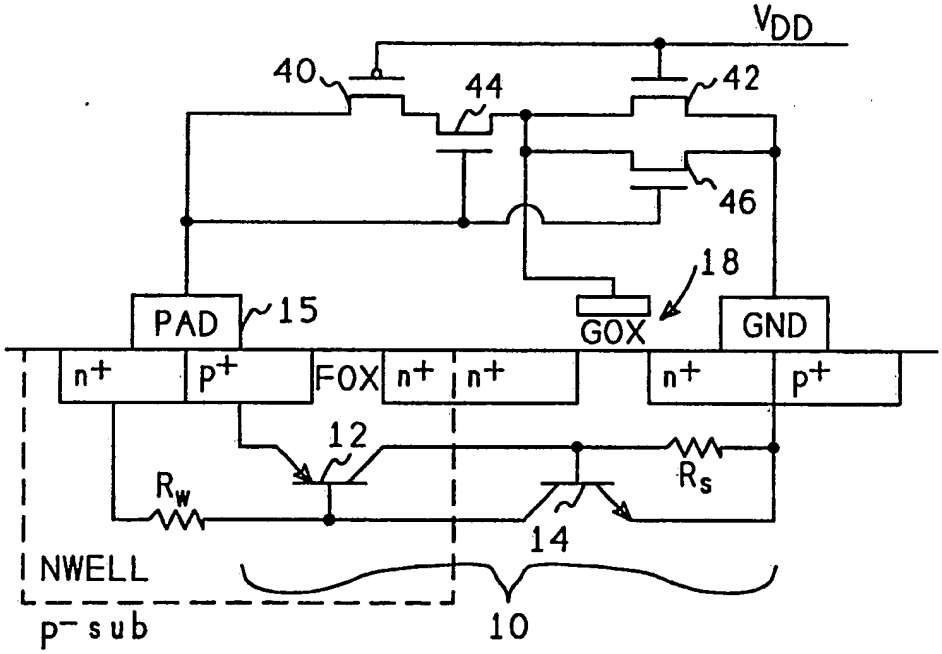

$V_{DD}$
40
44
42
46
18
PAD
15
GOX
GND
n+
p+
FOX
n+
n+
n+
p+
12
$R_w$
$R_s$
14
NWELL
$p^-$ sub
10

FIG. 4(b)

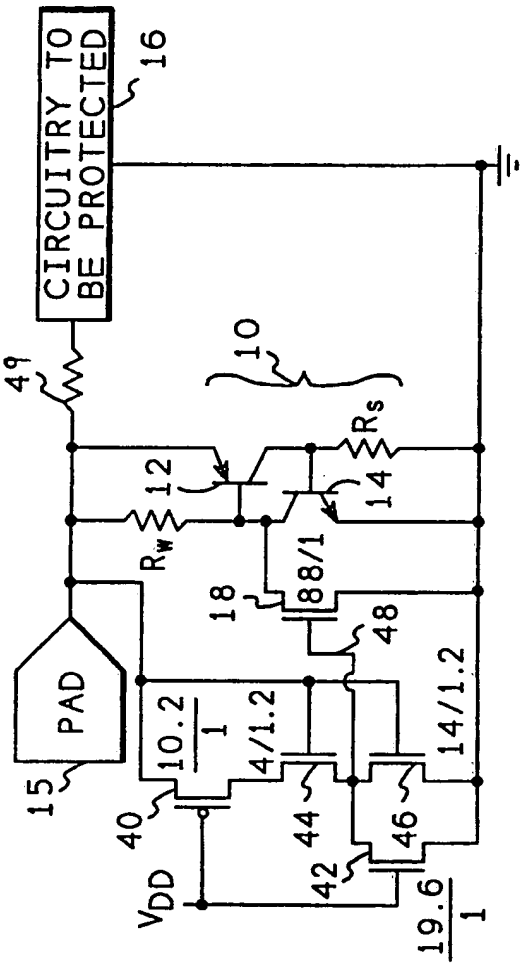

CIRCUITRY TO BE PROTECTED
16
49
10
$R_s$
12
14
$R_w$
88/1
18
48
PAD
15
10.2/1
4/1.2
14/1.2
40
44
46
42
$V_{DD}$
19.6/1

FIG. 5(a)

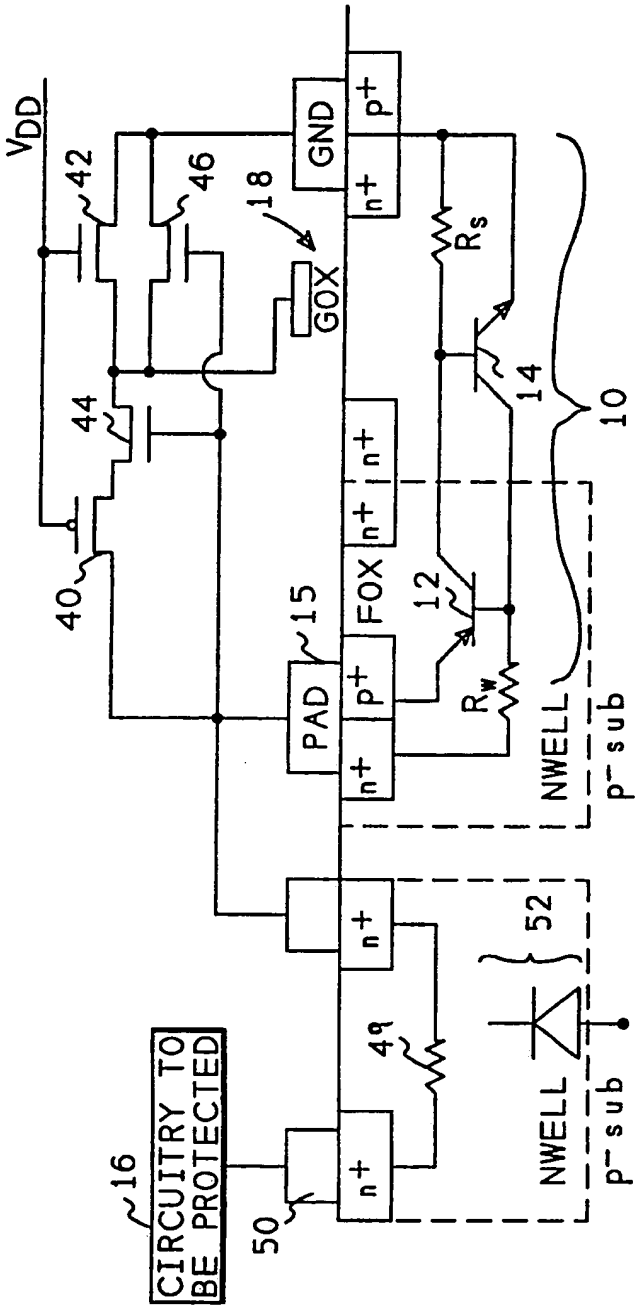

VDD
42
46
18
GND
p+
n+
GOX
Rs
44
14
10
40
n+
n+
FOX
12
15
PAD
p+
Rw
n+
NWELL
p- sub
52
49
n+
NWELL
p- sub
16
CIRCUITRY TO BE PROTECTED
50

FIG. 5(b)

# Electrostatic Discharge Protection Circuit

This invention relates to electronic circuits and more particularly to a circuit for protecting integrated circuits from electrostatic discharge. The preferred embodiment relates to an electrostatic discharge protection circuit having a trigger circuit for triggering a silicon controlled rectifier (SCR) circuit which uses the SCR latchup effect present in CMOS processes to divert the electrostatic discharge current pulse away from sensitive integrated circuit structures.

Electrostatic discharge (ESD) causes substantial damage to integrated circuits during and after the chip manufacturing process. ESD events are particularly troublesome for CMOS chips because of their low power requirements and extreme sensitivity. On-chip ESD protection circuits for CMOS chips is essential. Generally, such circuits require a high failure threshold, a small layout size and a low RC delay so as to allow high speed applications. However, such ESD protection circuits have heretofore been difficult to design.

Previously, resistors and diodes were used in CMOS ESD protection circuits, but such resistors and diodes have been gradually replaced by 3-layer devices such as field-oxide MOSFETs, gate-oxide MOSFETs and parasitic NPN or PNP bipolar junction transistors in CMOS technologies. Others have used a parasitic 4-layer PNPN device known as a silicon control rectifier to protect the chip against the damages caused by ESD events.

Due to its high current sinking/sourcing capability, very low turn-on impedance, low power dissipation, and large physical volume for heat dissipation, parasitic lateral SCR devices have been recognized in the prior art as one of the most effective elements in CMOS on-chip ESD protection circuits. However, there is a major disadvantage when using the parasitic SCR device in ESD protection circuits in that the SCR device has a high trigger voltage. To perform ESD protection, the trigger voltage of an ESD protection circuit must be less than the voltage that can damage the input buffer or output driver. The typical trigger voltage of a parasitic lateral SCR device in the ESD protection circuits fabricated by the advanced 1$\mu$m CMOS process with highly doped drain and silicided diffusion is about 50 volts if the space from its anode to its cathode is 6$\mu$m.

Unfortunately, with such a high trigger voltage, the lateral SCR device cannot be used as the only protection element. Figs. 1(a) and 1(b) illustrate an ESD protection circuit having an SCR structure. Fig. 1(a) illustrates the circuit diagram, while Fig. 1(b) illustrates the corresponding substrate. The ESD protection device illustrated in Figs. 1(a) and 1(b) includes an SCR device 10 comprising cross-coupled bipolar PNP transistor 12 and NPN transistor 14 connected between an input/output pad 15, on the integrated circuit 16 to be protected, and the chip ground (also substrate) of the integrated circuit 16. The resistance $R_s$ of the P-substrate in which the SCR 10 is formed is illustrated along with the well resistance $R_w$, which establishes a threshold current that must be reached before the SCR device 10 may be activated. As illustrated in Figs. 1(a) and 1(b), an NMOS trigger FET 18 is further provided for lowering the triggering voltage of the SCR 10 to the breakdown voltage of the trigger FET 13.

The ESD protection circuit illustrated in Figs. 1(a) and 1(b) thus requires that a trigger device such as NMOS trigger FET 18 be subjected to junction breakdown conditions before the SCR 10 may be activated. In particular, enough current must flow through the NMOS trigger FET 18 to initiate latchup by the SCR device 10. However, since the circuitry 16 being protected can also experience junction breakdown, there is no mechanism in the circuit of Fig. 1 to ensure that enough current will flow through the NMOS trigger FET 18 to initiate latchup. Furthermore, there is no assurance that device breakdown effects such as bipolar snapback will result in all the ESD current being absorbed by the ESD protection circuitry rather than the output circuit.

During operation of the circuit of Fig. 1, the NMOS trigger FET 18 operates in the junction breakdown condition to pull current through the well resistor $R_w$. This breakdown voltage is approximately equal to the breakdown voltage of the circuitry to be protected, and, as just noted, it is impossible in such a circuit to ensure that the circuitry 16 to be protected will not conduct significant amounts of current due to device breakdown. It is also not possible to ensure that the circuitry 16 to be protected will not "steal" the current from the SCR device 10, thereby inhibiting the SCR 10 from latching up and absorbing the majority of the ESD event energy. Fig. 1 also shows a fixed resistor 17 used to limit current into the circuit to be protected. This fixed resistor has the disadvantage that it must be of a high value to prevent damage in a discharge event, but it must be of a low value to allow the circuit to properly drive a signal to the pad.

Figs. 2(a) and 2(b) illustrate an ESD protection circuit of the type illustrated in Fig. 1 except that an NMOS FET 20 is added

for lowering the breakdown voltage by floating the gate of NMOS trigger 18 when chip power $V_{DD}$ is low. Fig. 2(a) illustrates the circuit diagram, while Fig. 2(b) illustrates the corresponding substrate. As illustrated, the NMOS FET 20 is responsive to $V_{DD}$ to float the gate of the NMOS trigger FET 18 when the circuitry 16 to be protected is not powered up. Once powered up ($V_{DD}$ goes high) the gate of the trigger FET 18 is grounded so as to raise the breakdown voltage of trigger FET 18, thus minimizing the effect of the protection circuitry on the operation of the circuitry 16 to be protected. However, in the circuitry of Figs. 2(a) and 2(b), latching by the SCR device 10 still relies upon the breakdown of the NMOS trigger FET 18 for initiation of latchup and is still susceptible to current "stealing" by the circuitry 16, which will also have floating gates. Thus, the aforementioned problems have not been overcome by the circuit of Fig. 2.

The present invention seeks to provide an improved electrostatic discharge protection circuit.

According to an aspect of the present invention, there is provided an electrostatic discharge protection circuit for protecting an integrated circuit from an ESD event at an input/output pad connected to said integrated circuit, said ESD protection circuit comprising: a silicon controlled rectifier (SCR) circuit connectable between said input/output pad and a device ground of said integrated circuit for absorbing current created by an ESD event at said input/output pad; and triggering means for actively triggering said SCR circuit to absorb current created by an ESD event, said triggering means comprising a trigger FET for activating said SCR circuit and adjustable threshold means responsive to said ESD event at said input/output pad for applying a trigger voltage to a gate of said trigger FET so

as to activate said SCR circuit upon receipt of said ESD event at said input/output pad independent of a junction breakdown of said trigger FET.

It is possible with the invention to provide an ESD protection circuit which will enable the SCR to latch independently of the breakdown effects of the NMOS trigger FET. It is also possible to provide a circuit that can control the amount of voltage necessary to initiate SCR latchup.

The circuit can divert an electrostatic discharge current pulse away from sensitive integrated circuit structures.

Preferably, the threshold voltage of such a discharge can be adjusted during fabrication of the integrated circuit to allow use in different applications.

In a preferred embodiment, there is provided an ESD protection circuit that uses the well-known SCR latchup effect present in CMOS processes to divert the ESD current pulse away from sensitive circuit structures. In preferred embodiments, this is accomplished using an inverter trigger device, with an output voltage divider, that is responsive to an ESD event on the input/output pad of the integrated circuit being protected. This feature can enable the SCR to absorb a high current pulse on the CMOS pad structures caused by an ESD event, while also preventing the circuit from latching when an ordinary CMOS voltage is applied to the pad while the circuit being protected is unpowered.

The ESD protection circuit can ensure that the SCR will latch independent of breakdown effects so as to protect the integrated circuits from and ESD event at input/output pads connected to the integrated circuits, while also allowing

adjustment of the threshold voltage at which latchup occurs. This adjustment can be performed by varying the sizes of two FETs used as the voltage divider.

The ESD protection circuit can also provide a well resistor formed between the pad and the circuit to be protected, which provides additional protection. Because the well resistor forms a diode with the substrate, a depletion region will be formed during an ESD event, and this depletion region increases the resistance of the well resistor to provide additional protection for the circuit.

An embodiment of the present invention is described below, by way of example only, with reference to the accompanying drawings, in which:

Figures 1(a) and 1(b) show a prior art ESD protection circuit comprising an SCR which is triggered by the junction breakdown of an NMOS trigger FET;

Figures 2(a) and 2(b) show a prior art ESD protection circuit comprising an SCR which is triggered by the junction breakdown of an NMOS trigger FET having a floating gate;

Figures 3(a) and 3(b) show an embodiment of an ESD protection circuit comprising an SCR with an inverter trigger responsive to an ESD event on the input/output pad;

Figures 4(a) and 4(b) show another embodiment of an ESD protection circuit comprising an SCR with an inverter trigger responsive to and ESD event and further comprising a voltage divider circuit on the output of the inverter trigger; and

Figures 5(a) and 5(b) show another embodiment of an ESD protection circuit comprising an SCR with an

inverter trigger responsive to an ESD event and further comprising a well resistor between the protection circuitry and the circuit being protected.

Figures 3 and 4 show an electrical discharge protection circuit for protecting integrated circuits in accordance with the techniques of the invention. In each of the Figures, part (a) illustrates the circuit diagram while part (b) illustrates the corresponding substrate. In addition, the illustrated FETs are given width/length values in the drawings which correspond to the sizes of these elements in a preferred embodiment. However, it will be appreciated by those of ordinary skill in the art that FETs of other sizes may be used and that the description given herein with respect to those Figures is for exemplary purposes only and thus, not intended in any way to limit the scope of the invention.

Figs. 3(a) and 3(b) illustrate an ESD protection circuit comprising an SCR with inverter trigger. This embodiment differs from that of prior art Fig. 1 in that a trigger circuit is provided comprising an NMOS trigger FET 18 and an inverter 30 which drives the gate of the NMOS trigger FET 18 in response to an ESD even at the input/output pad 15. Inverter 30 receives its power from the input/output pad 15, which is powered by the ESD event. The signal into the inverter 30, $V_{DD}$, is the chip global positive power supply, while the ground is the chip substrate.

Fig. 3(b) illustrates that the inverter 30 comprises a PFET 40 and an NFET 42 connected in series between the pad 15 and circuit ground. $V_{DD}$ is connected to the gate of both the FETs and the output comes from the connection between the two FETs. This output is connected to the gate of NMOS trigger FET 18.

During as ESD event, the chip global power supply $V_{DD}$ is at ground, therefore, the gates of PFET 40 and NFET 42 are both connected to ground. As the electrostatic discharge into the input/output pad 15 progresses, the voltage on the input/output pad 15 rises and as it reaches approximately 2 volts it causes PFET 40 to start conducting, therefore, the source of PFET 40 also rises to approximately 2 volts and this voltage, which is connected to the gate of NMOS trigger FET 18, causes NMOS trigger FET 18 to conduct which causes the SCR to latch.

Under certain conditions, however, this latching can occur to cause an undesirable side effect. For example, where two integrated circuit devices are interconnected, and a CMOS output connection from the first integrated circuit device is connected to input/output pad 15 contained in the second integrated circuit device, a problem occurs if the first device is powered up and the second device is not powered up. When the second device is not powered up, $V_{DD}$ will be at zero volts, however, the connection from the first device, connected to input/output pad 15, may be at 5 volts, since it is connected to an output of a powered up device (the first device), and 5 volts is a normal voltage for the output of a powered up device. In this condition, if the first device supplies sufficient current, SCR 10 will latchup. Therefore, if the second device is subsequently powered up, the circuit can remain latched and operate incorrectly. Thus, it can be seen that while a very low trigger voltage of 2 volts is desirable when the circuit is unconnected, it may be too low for the circuit when connected to a device with a separate $V_{DD}$.

Fig. 4 shows the circuit of the preferred embodiment of the present invention which overcomes the undesirable side effect of

the circuit of Fig. 3 by allowing the trigger voltage to be adjusted during the fabrication of the integrated circuit. Referring now to Fig. 4(a), the inverter 30 from Fig. 3 is shown comprising the PFET 40 and the NFET 42. A pair of NFETs 44 and 46 form a voltage divider between the source of PFET 40 and circuit ground. By adjusting the sizes of the NFETs 44 and 46, the trigger voltage output 48, between the source of NFET 44 and the drain of NFET 46, can be adjusted to a higher voltage. The NFETs 44 and 46 could be designed, for example, to require 7 volts on the pad 15 in order to produce a trigger voltage output 48 large enough to cause the SCR to latch, thus preventing the above described undesirable side effect between two connected devices with separate $V_{DD}$s.

In operation, if the circuit of Fig. 4 is not powered up, $V_{DD}$ is at zero volts. During an ESD event, the electrostatic discharge into the input/output pad 15 progresses, the voltage on the input/output pad rises so as to turn on PFET 40. As discussed above, this turn-on can occur as low as approximately 1 volt. The source of PFET 40, however, is connected to circuit ground through the voltage divider comprising NFET 44 and NFET 46. NFET 42 will be cut off since its gate is connected to $V_{DD}$. Thus, as the source of PFET 40 rises to above one volt when PFET 40 turns on, the output 48 will be lower than the source of FET 8 because of the effect of the voltage divider formed by NFET 44 and NFET 46. As the voltage on input/output pad 15 continues to rise, at some voltage determined by the sizes of NFET 44 and NFET 46, the voltage on signal 48 will rise to a level sufficient to turn NMOS trigger FET 18 on, which causes the SCR 10 to latch.

If the sizes of NFET 44 and NFET 46 are selected such that the voltage on input/output pad 15 must be 7 volts or higher before the

latchup occurs, the undesirable side effect described above, wherein a first device is powered up and a second device is not powered up, will not cause a trigger event. As described above, if the first device is powered up, the voltage on pad 15 will only be 5 volts, and because of the voltage divider circuit formed by NFET 44 and NFET 46, the voltage on signal 48 will be too low to cause NMOS trigger FET 18 to turn on.

Once the circuit of Fig. 4(a) is powered up, $V_{DD}$ goes to 5 volts which causes NFET 42 to turn on and ground the voltage on signal on 48, to prevent any later latchup. Thus, it can be seen that the voltage divider circuit formed by NFET 44 and NFET 46 allows the trigger voltage to be adjusted wherein the voltage can be adjusted high enough to prevent unwanted trigger events, yet still remain low enough to cause the SCR 10 to trigger in an actual ESD discharge event. Furthermore, the circuit of the present invention provides a positive control of the trigger voltage rather than depending upon junction breakdown conditions as in the prior art.

Although the circuit of Fig. 4 is shown using NFETs for the voltage divider, those of ordinary skill in the art will recognize that PFETs could also be used, as could resistors formed within the integrated circuit.

Figs. 5(a) and 5(b) show the circuit of Figs. 4(a) and 4(b), respectively, and further show a well resistor 49. The well resistor 48 provides additional protection for the circuit 16, but operates significantly different from the fixed resistor 17, shown above in Fig. 1.

As shown in Fig. 5(b), the well resistor 49 is formed by an n-well within the substrate, thus it is made of semiconductor

material. Because the well resistor 49 is made of n-type semiconductor material, and it is constructed within the p-substrate, a diode 52 exists between these two types of material. When an ESD event occurs, voltage will build on the pad 15, and this voltage will reverse bias diode 52. Because of the reverse bias, diode 52 will form a depletion region, and the size of this depletion region will be dependent upon the ESD voltage. As the ESD voltage increases, the depletion region gets larger, which increases the resistance of the well resistor 49. As the ESD voltage continues to increase, the depletion region will become so large as to "pinch off" the well resistor, limiting current flow into the circuity to be protected 16, thus providing additional protection.

During normal operation, the normal signal voltages on pad 15 are low enough to keep the depletion region very small, thus providing a low resistance to signal flow through the pad 15.

Therefore, under normal operation, the well resistor 49 is a very small resistance allowing signals to flow through the pad 15. During an ESD event, however, when the voltage on pad 15 increases far beyond normal operating voltages, the well resistor becomes a higher value and eventually limits the current flow into the circuit to be protected 16 to provide additional protection.

The well resistor could also be added to the circuit of Figs. 3(a) and 3(b) to provide protection in the same manner as discussed above with respect to Figs 4(a) and 4(b).

The disclosures in United States patent application no. 08/149,858, from which this application claims priority, and in the abstract accompanying this application are incorporated herein by reference.

CLAIMS

1. An electrostatic discharge (ESD) protection circuit for protecting an integrated circuit from an ESD event at an input/output pad connected to said integrated circuit, said ESD protection circuit comprising:

a silicon controlled rectifier (SCR) circuit connectable between said input/output pad and a device ground of said integrated circuit for absorbing current created by an ESD event at said input/output pad; and

triggering means for actively triggering said SCR circuit to absorb current created by an ESD event, said triggering means comprising a trigger FET for activating said SCR circuit and adjustable threshold means responsive to said ESD event at said input/output pad for applying a trigger voltage to a gate of said trigger FET so as to activate said SCR circuit upon receipt of said ESD event at said input/output pad independent of a junction breakdown of said trigger FET.

2. A circuit according to claim 1, wherein said adjustable threshold means comprises:

control means powered by an ESD event for conducting an ESD voltage to an output of the control means; and

voltage divider means connected between said control means output and circuit ground and including a voltage reduced output connected to a gate of said trigger FET, whereby a voltage output to said trigger FET is reduced by said voltage divider means before being applied to said gate of said trigger FET.

3. A control circuit according to claim 2, wherein said control means includes an inverter powered by an ESD event, said voltage divider means being connected between the output of the inverter and circuit ground.

4. A circuit according to claim 2 or 3, wherein said control means includes a control FET powered by an ESD event, said voltage divider means being connected between the output of said control FET and circuit ground.

5. A circuit according to claim 2, 3 or 4, comprising a grounding FET for grounding said voltage reduced output when power is applied to said integrated circuit.

6. A circuit according to any one of claims 2 to 5, wherein said voltage divider means comprises a pair of FETs connected in series.

7. A circuit according to claim 2 or 3, wherein said pair of FETs are NFETs or PFETs.

8. A circuit according to any preceding claim, comprising a well resistor between said input/output pad and circuitry to be protected within said integrated circuit.

9. An electrostatic discharge protection circuit substantially as hereinbefore described with reference to and as illustrated in Figures 3, 4 or 5 of the accompanying drawings.

| Patents Act 1977<br>Examiner's report to the Comptroller under Section 17<br>(The Search report) 14 | Application number<br>GB 9422471.4 |
|---|---|
| **Relevant Technical Fields**<br>(i) UK Cl (Ed.N) H1K-KGPE; H2H-HAPC<br>(ii) Int Cl (Ed.6) H01L; H02H | Search Examiner<br>S J DAVIES<br>Date of completion of Search<br>1 FEBRUARY 1995 |
| **Databases** (see below)<br>(i) UK Patent Office collections of GB, EP, WO and US patent specifications.<br>(ii) ONLINE WPI | Documents considered relevant following a search in respect of Claims :-<br>ALL |

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